Sheet 1 of 3

U.S. Department of Commerce, Patent and Trademark Office				Attorne	Attorney Docket No.		Serial No.		
					SUN04	SUN040292 10/790,650			
INFORMATION DISCLOSURE STATEMENT BY APPLICANT					Applica	Applicant(s)			
(Use several sheets if necessary)					Harinat	Harinath B. Kamepalli et al.			
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32				March 1	1, 2004	Unkad	Unknown		
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Initial PD	AA	Number 6,634,012	Date 10/14/2003	Name Zhong et al.	Class 716	Subclass 5	If Appro	priate	
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PD	AR	Takahashi, Tsuyoshi, et al., "Design Flow and Design Environment for System LSIs," Hitachi Review Vol. 48 (1999) No. 2, pp. 87-93							
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Examiner PAUL DINH Date				ate Considered 7/13/05					
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U.S. Department of Commerce, Patent and Trademark Office					Attorne	Attorney Docket No.		Serial No.	
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:	OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)								
PD	AR	http://www.synopsys.com/products/acmgr/innlo/, "Former InnoLogic Systems Products"							
PD	AS	http://www.synopsys.com/products/acmgr/innlo/espcv.html, "ESP-CV"							
PD	АТ	http://www.synopsys.com/products/acmgr/innlo/esplv.html, "ESP-LV"							
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your communication to applicant.									

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U.S. Department of Commerce, Patent and Trademark Office					Attorne	Attorney Docket No.		Serial No.	
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PD	AR	http://www.synopsys.com/products/acmgr/innlo/espbv.html, "ESP-BV"							
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Examiner	Examiner PAUL DINH Date Considered 7/13/05								
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if not in conformance and not considered. Include copy of this form with your communication to applicant.									